WHAT IS CLAIMED IS:

1. A phase detector operable in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

at least one first flip flop operable to sample said second clock signal with a rising edge of said first clock signal, said at least one first flip flop thereby operating to generate a one-to-zero transition in a first sampled clock signal following coincident rising edges between said first and second clock signals; and

at least one second flip flop operable to sample said second clock signal with a falling edge of said first clock signal, said at least one second flip flop operating to generate a zero-to-one transition in a second sampled clock signal following said coincident rising edges between said first and second signals,

wherein a movement in one of said one-to-zero and zero-to-one transitions is operable to track a movement in said coincident rising edges corresponding to a phase difference between said first and second clock signals.

2. The phase detector as recited in claim 1, wherein said at least one first flip flop comprises two flip flops operable to sample said second clock signal with a rising edge of said first clock signal.

3. The phase detector as recited in claim 1, wherein said at least one second flip flop comprises two flip flops operable to sample said second clock signal with a falling edge of said first clock signal.

4. The phase detector as recited in claim 3, further comprising a third flip flop operable to sample an output of said two flip flops using said rising edge of said first clock signal.

5. The phase detector as recited in claim 1, wherein said sampled clock signals are operable to be forwarded to a core clock synchronizer controller.

6. The phase detector as recited in claim 1, wherein said sampled signals are operable to be forwarded to a cycle and sequence generator.

7. The phase detector as recited in claim 1, wherein said sampled clock signals are operable to be forwarded to a skew state detector.

8. The phase detector as recited in claim 1, wherein said first clock signal is a core clock signal.

9. The phase detector as recited in claim 1, wherein said second clock signal is a bus clock signal.

10. A phase detection method operable in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

sampling said second clock signal with a rising edge of said first clock signal to generate a first sampled clock signal;

sampling said second clock signal with a falling edge of said first clock signal to generate a second sampled clock signal; and

detecting a phase difference between said first clock signal and said second clock signal by tracking movement in one-to-zero or zero-to-one transitions in said sampled clock signals.

11. The method as recited in claim 10, wherein the operation of sampling said second clock signal with a rising edge of said first clock signal comprises sampling a bus clock signal with a rising edge of a core clock signal.

12. The method as recited in claim 10, wherein the operation of sampling said second clock signal with a falling edge of said first clock signal comprises sampling a bus clock signal with a falling edge of a core clock signal.

13. The method as recited in claim 10, further comprising the operation of forwarding at least one of said sampled clock signals indicative of the detected phase difference to a core clock synchronizer controller.

14. The method as recited in claim 10, further comprising the operation of forwarding at least one of said sampled clock signals indicative of the detected phase difference to a cycle and sequence generator.

15. The method as recited in claim 10, further comprising the operation of forwarding at least one of said sampled clock signals indicative of the detected phase difference to a skew state detector.

16. A phase detector operable in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

means for sampling said second clock signal with a rising edge of said first clock signal to generate a first sampled clock signal;

means for sampling said second clock signal with a falling edge of said first clock signal to generate a second sampled clock signal; and

means for detecting a phase difference between said first clock signal and said second clock signal by tracking movement in one-to-zero or zero-to-one transitions in said sampled clock signals.

17. The phase detector as recited in claim 16, wherein said means for sampling said second clock signal with a rising edge of said first clock signal comprises means for sampling a bus clock signal with a rising edge of a core clock signal.

18. The phase detector as recited in claim 16, wherein said means for sampling said second clock signal with a falling edge of said first clock signal comprises means for sampling a bus clock signal with a falling edge of a core clock signal.

19. The phase detector as recited in claim 16, further comprising means for forwarding at least one of said sampled clock signals indicative of the detected phase difference to a core clock synchronizer controller.

20. The phase detector as recited in claim 16, further comprising means for forwarding at least one of said sampled clock signals indicative of the detected phase difference to a cycle and sequence generator.

21. The phase detector as recited in claim 16, further comprising means for forwarding at least one of said sampled clock signals indicative of the detected phase difference to a skew state detector.